4. Clampers:

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal. Additional shifts can also be obtained by introducing a dc supply to the basic structure.

The chosen resistor and capacitor of the network must be chosen such that the time constant determined by **τ = RC** is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in **five-time** constants.

The simplest of clamper networks is provided in **Figure (4.1)**. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

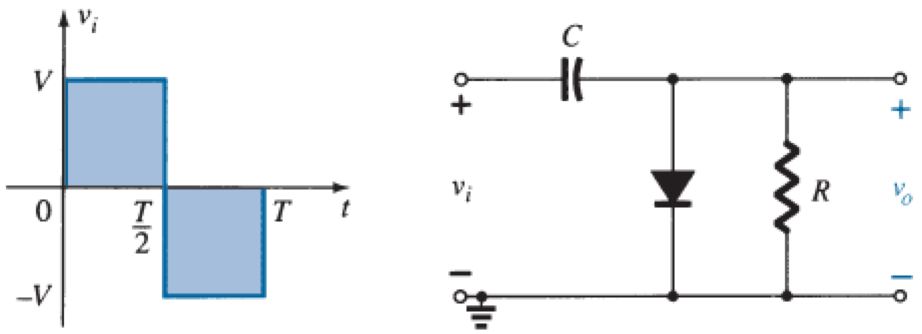
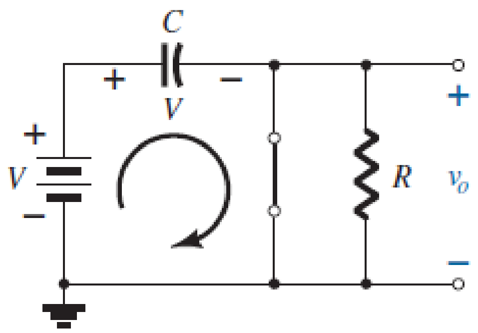
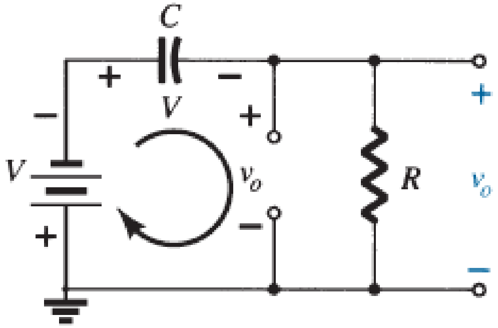


Figure (4.1): Clamper.

During the interval (0 to T/2) the diode is in short circuit (on state) shorting out the effect of the resistor R, thus the capacitor will charge to V very quickly and $V_o = 0$, as shown in Figure below.



During the interval (T/2 to T) the diode is in open circuit (off state) now R is back in the network.

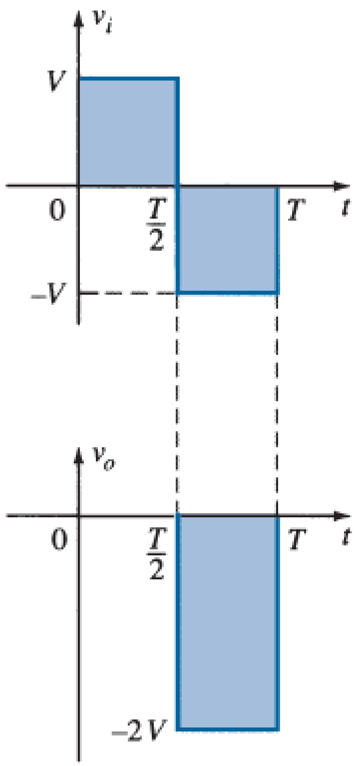


The capacitor holds the charge and therefor voltage (V=Q/C). Thus, by using Kirchhoff's voltage law around the input loop results in:

$$-V - V - V_o = 0$$

$$V_o = -2V$$

The output signal is as shown in Figure below:



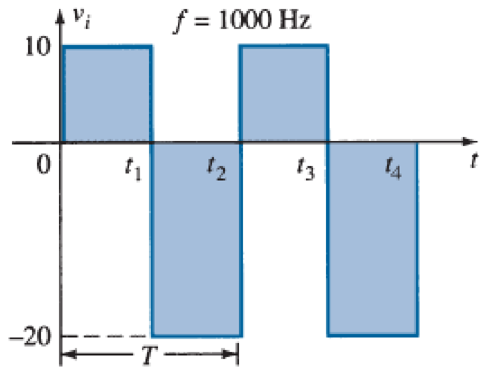
For clamping networks, the total swing of the output is equal to the total swing of the input signal.

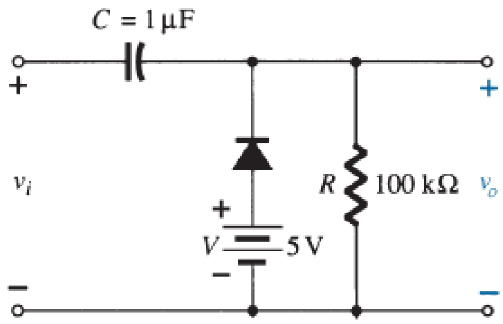
The following steps may be used for analyzing clamping networks:

1. Start the analysis from the period of the input signal that will forward bias the diode.
2. During this period assume that the capacitor will charge up to a level determined by the voltage across the capacitor in its equivalent open-circuit state.

3. Assume that during the period the diode is an open circuit (off state) the capacitor will hold on its charge and therefor voltage.
4. Applying Kirchhoff's voltage law to determine V_o for both state on and off.
5. The general rule that the swing of the output signal must match the swing of the input signal.

Example 1: Determine V_o for the network of Figure below for the input indicated.

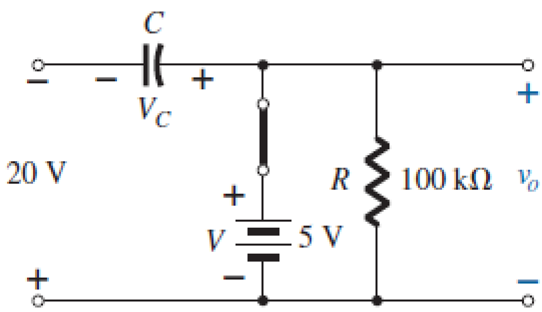




Solution:

Note that the frequency is 1000 Hz, resulting in a period of T= 1/f =1/1000Hz =1 ms and an interval of 1/2T=1/(2×1000) = 0.5 ms between levels.

The analysis will begin with the period t_1 to t_2 of the input signal since the diode is in its short-circuit state. For this interval, the network will appear as shown in Figure below.

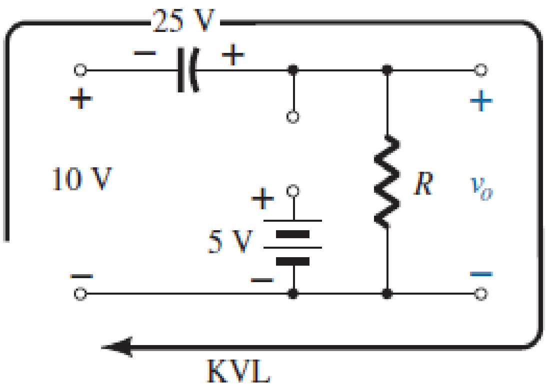


The output is across R, but it is also directly across the 5V battery. The result is $Vo\ = V - V_D =\ 5V$ for this interval. Applying Kirchhoff's voltage law around the input loop will result in: $-V_i + V_c + V_D - V = 0$

$$-20v + V_c + 0v - 5v = 0$$

$$V_c = 25\ volts$$

The capacitor will therefore charge up to 25 V. For the period t_2 to t_3, the network will appear as shown in Figure below.



The open-circuit equivalent for the diode will remove the 5V battery from having any effect on V_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in:

$+V_i + V_c - V_o = 0$

$+10v + 25v - V_o = 0$

$V_o = 35\ volts$

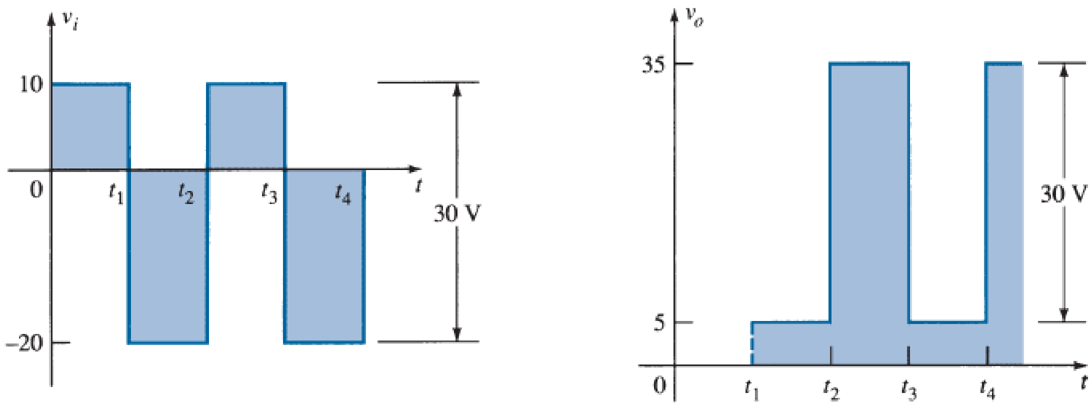
The time constant of the discharging network is determined by the product RC:

$\tau = RC = 100k\Omega \times 0.1\mu F = 0.01\ sec = 10\ msec$

The total discharge time is therefore $5\tau\ =\ 5 \times 10\ msec =\ 50\ msec.$

Since the interval t_2 to t_3 will only last for 0.5 msec, i.e. the capacitor will hold its voltage during the discharge period between pulses of the input signal.

The resulting output appears in Figure below with the input signal.



Example 2: **Repeat Example1 using a silicon diode with V_T = 0.7 V.**

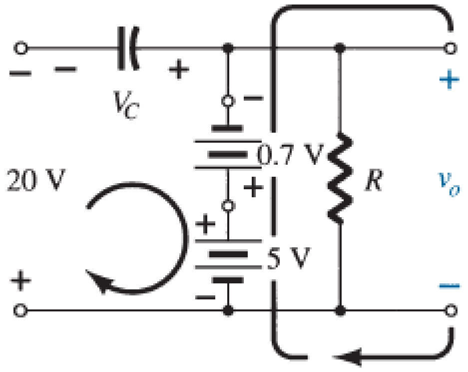
Solution:

For the short-circuit state V_o can be determined by Kirchhoff's voltage law in the output section:

$+V - V_D - V_o = 0$

$+5v - 0.7v - V_o = 0$

$V_o = 5v - 0.7v = 4.3v$



For the input section Kirchhoff's voltage law results in:

$-V_i + V_c + V_D - V = 0$

$-20 + V_c + 0.7v - 5v = 0$

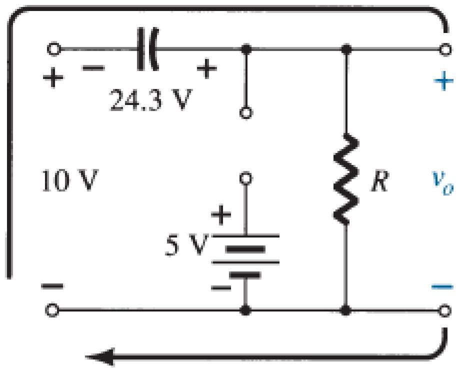
$V_c = 24.3v$

For the period t_2 to t_3 the network as in Figure below, applying Kirchhoff's voltage law:

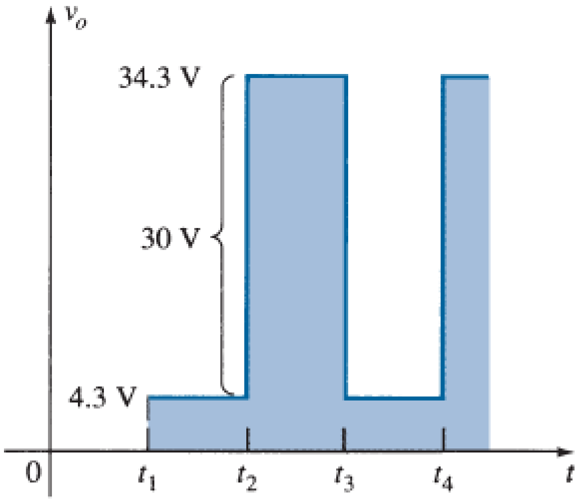
$+V_i + V_c - V_o = 0$

$+10v + 24.3v - V_o = 0$

$V_o = 34.3v$



The resulting output appears in Figure below:



A number of clamping circuits shown in **Figure (4.2)**:

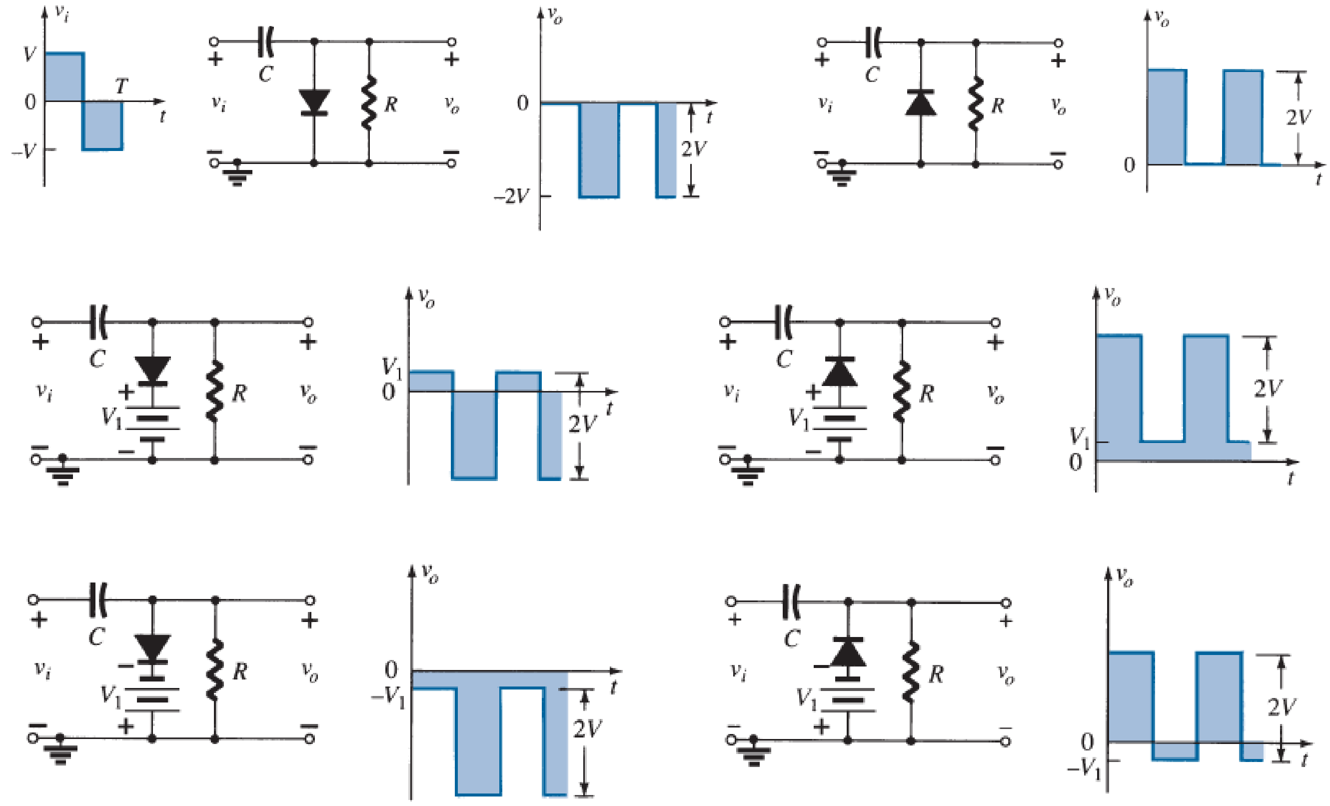


Figure (4.2): Clamping circuits with ideal diodes (5τ = 5RC >> T/2).